

Contents

INTRODUCTION	1
OVERVIEW	1
WHAT'S INCLUDED	1
FACTORY DEFAULT SETTINGS.....	1
CARD SETUP	2
ADDRESS SELECTION.....	2
PORT ENABLE DISABLE	3
TRANSMIT CLOCK / RS-485 ENABLE HEADER E8	4
DMA CHANNEL SELECTION HEADERS E4 - E7.....	5
DMA JUMPER OPTION TABLES	6
No DMA	6
Single Channel DMA (Half Duplex Only).....	6
Two DMA Channels Selected.....	6
Full Duplex Channel A and B with four DMA Channels	7
Full Duplex Channel A only	7
Full Duplex Channel B only	7
DMA ENABLE HEADER E2	8
IRQ SELECTION HEADER E3.....	9
IRQ MODE HEADER E1	9
INSTALLATION	10
CABLING OPTIONS	10
TECHNICAL DESCRIPTION	11
FEATURES.....	11
Internal Baud Rate Generator	11
PROGRAMMING THE OMG-ACB-530.....	12
Control/Status Port	12
Software Examples	12
DMA TERMINAL COUNT	13
CONNECTOR P1 AND P2 PIN ASSIGNMENTS	14
RS-530/422/485 Line Termination	14
SPECIFICATIONS	15
ENVIRONMENTAL SPECIFICATIONS	15
POWER CONSUMPTION	15
MEAN TIME BETWEEN FAILURES (MTBF).....	15
PHYSICAL DIMENSIONS.....	15
APPENDIX A - TROUBLESHOOTING	16
APPENDIX B - HOW TO GET ASSISTANCE	17

APPENDIX C - ELECTRICAL INTERFACE	18
RS-422.....	18
RS-530.....	18
RS-449.....	18
RS-485.....	19
APPENDIX D - DIRECT MEMORY ACCESS	20
APPENDIX E - ASYNCHRONOUS AND SYNCHRONOUS COMMUNICATIONS	21
ASYNCHRONOUS COMMUNICATIONS	21
SYNCHRONOUS COMMUNICATIONS	23
APPENDIX F - ACB DEVELOPER TOOLKIT DISKETTE AND ACB RESOURCE KIT	25
APPENDIX G - SILK-SCREEN	26
APPENDIX H - COMPLIANCE NOTICES	27
FEDERAL COMMUNICATIONS COMMISSION STATEMENT	27
EMC DIRECTIVE STATEMENT.....	27
WARRANTY.....	28

Figures

Figure 1 - Address Selection Table.....	2
Figure 2 - DIP-switch Illustration.....	2
Figure 3 - Clock Option / RS-485 Enable Selection Header E8	4
Figure 4 - DMA Selection Headers E4 - E7	5
Figure 5 - DMA Enable Header E2.....	8
Figure 6 - IRQ Header E3	9
Figure 7 - IRQ Mode Header	9
Figure 8 - Asynchronous Communications Bit Diagram	22
Figure 9 - Synchronous Communications Bit Diagram.....	23

Introduction

Overview

The Omega Engineering **OMG-ACB-530** provides the PC with two high-speed RS-530/422/485 synchronous/asynchronous ports. The **OMG-ACB-530** can be used in a variety of sophisticated communications applications such as SDLC, HDLC, X.25, Bi-Sync, Mono-Sync, and high-speed asynchronous.

What's Included

The **OMG-ACB-530** is shipped with the following items. If any of these items are missing or damaged, contact the supplier.

- **OMG-ACB-530** Serial Interface Adapter
- 3.5" ACB Developers Toolkit Diskette
- Channel B Interface Cable
- User Manual

Factory Default Settings

The **OMG-ACB-530** factory default settings are as follows:

Base Address	DMA Port A	DMA Port B	IRQ	Electrical Specification
238	TX: 1 / RX: 3	TX: 0 / RX: 2	5	RS-530/422

To install the **OMG-ACB-530** using factory default settings, refer to the section on Installation.

For your reference, record installed **OMG-ACB-530** settings below:

Base Address	DMA Port A	DMA Port B	IRQ	Electrical Specification

Card Setup

The **OMG-ACB-530** contains several jumper straps for each port, which must be set for proper operation.

Address Selection

The **OMG-ACB-530** occupies 8 consecutive I/O locations. A DIP-switch (SW1) is used to set the base address for these locations. The **OMG-ACB-530** can reside in any I/O location between 100 and 3F8 Hex. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	Binary	Switch Settings						
		1	2	3	4	5	6	7
	A9-----A0							
238-23F	1000111XXX	Off	On	On	On	Off	Off	Off
280-287	1010000XXX	Off	On	Off	On	On	On	On
2A0-2A7	1010100XXX	Off	On	Off	On	Off	On	On
2E8-2EF	1011101XXX	Off	On	Off	Off	Off	On	Off
300-307	1100000XXX	Off	Off	On	On	On	On	On
328-32F	1100101XXX	Off	Off	On	On	Off	On	Off
3E8-3EF	1111101XXX	Off	Off	Off	Off	Off	On	Off

Figure 1 - Address Selection Table

The following illustration shows the correlation between the DIP-switch setting and the address bits used to determine the base address. In the example below, the address 300 Hex through 307 Hex is selected. 300 Hex = 11 0000 0XXX in binary representation.

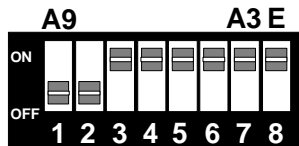


Figure 2 - DIP-switch Illustration

Note: Setting the switch 'On' or 'Closed' corresponds to a '0' in the address, while leaving it 'Off' or 'Open' corresponds to a '1'.

The relative I/O address of the **OMG-ACB-530** registers are as follows:

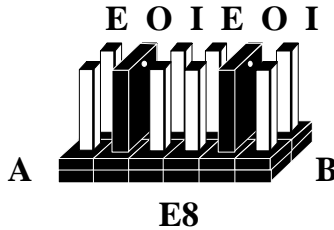
- Base+0 Channel A Data Port
- Base+1 Channel A Control Port
- Base+2 Channel B Data Port
- Base+3 Channel B Control Port
- Base+4 Board Control / Status Port
- Base+5 Reset TCIRQ

Port Enable Disable

The **OMG-ACB-530** can be enabled or disabled with switch position 8 on the DIP-switch. The port is enabled with the switch 'On' or 'Closed' and disabled when 'Off' or 'Open'.

Transmit Clock / RS-485 Enable Header E8

Header E8 sets the input/output clock modes for the transmit clock (TXC) and RS-485 driver enable. Please note that setting a jumper in position 'I' and position 'O' at the same time is not a valid option.



E	CH. A RTS Enable (For RS-485 Mode Only)
O	Transmit Clock Output Channel A
I	Transmit Clock Input Channel A
E	CH B. RTS Enable (For RS-485 Mode Only)
O	Transmit Clock Output Channel B
I	Transmit Clock Input Channel B

Figure 3 - Clock Option / RS-485 Enable Selection Header E8

In addition to RS-530, the **OMG-ACB-530** is capable of RS-422 and RS-485 communications. E8 position 'E' determines whether the RS-530 (and RS-485) transmit driver is enabled by the Enhanced Serial Communications Controller (ESCC) signal Request To Send (RTS) or always enabled. With the jumper installed, RTS enables the driver. Removing the jumper enables the driver regardless of RTS. This jumper should only be installed if you are running the board in a multi-drop polled environment such as RS-485, and you have software that knows how to 'talk' on the RS-485 bus. *For normal point-to-point RS-530 and RS-422, remove this jumper.*

DMA Channel Selection Headers E4 - E7

Headers E4 - E7 select **Direct Memory Access (DMA)** mode of operation. Each channel of the **Enhanced Serial Communications Controller (ESCC)** will function in half duplex or full duplex DMA modes. Full duplex means that DMA can be used for simultaneous transmit and receive. Half-duplex DMA means that you can either transmit, or receive with DMA, but not simultaneously. The 85230 has two signals that correspond to DMA request signals, WAIT/REQ and DTR/REQ. E5 & E7 correspond to WAIT/REQ and E4 & E6 correspond to DTR/REQ. WAIT/REQ and DTR/REQ can be programmed to serve as DMA request lines (DRQ) by setting the appropriate bits in Write Register 1 and Write Register 14 in the 85230. WAIT/REQ (E5 & E7) can be programmed for **Transmit** or **Receive** DMA transfers and DTR/REQ (E4 & E6) can be programmed for **Transmit Only**. For additional information on the programming of the 85230 please refer to the Zilog ESCC Users Manual. Please note that each DMA channel is selected by two jumpers. Only one DMA channel may be selected for each header block. Also refer to page 8 for the DMA enable (Software enable, Always enabled or Never enabled) option Header E2.

Note: If DMA is not used, remove all of the jumpers on E4 - E7 and install a jumper in position 'N' of E2

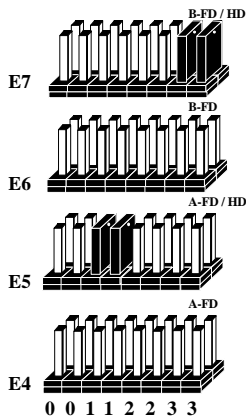


Figure 4 - DMA Selection Headers E4 - E7

E4 and **E5** select the **DMA Channel** for **Channel A** of the ESCC.

E6 and **E7** select the **DMA Channel** for **Channel B** of the ESCC.

Note: DMA Channel 0 is not available on 'XT' class machines, and DMA Channel 2 can only be used if the floppy disk DMA drivers are turned off. Please refer to the toolkit disk for software examples.

DMA Jumper Option Tables

The following tables show the jumper setting examples for each mode of DMA:

No DMA

Option	E4	E5	E6	E7
Ch.A No DMA; Ch.B No DMA	None	None	None	None

Single Channel DMA (Half Duplex Only)

Option	E4	E5	E6	E7
Ch.A DMA Ch.0 Half-Duplex Ch.B No DMA	None	00	None	None
Ch.A DMA Ch.1 Half-Duplex Ch.B No DMA	None	11	None	None
Ch.A DMA Ch.2 Half-Duplex Ch.B No DMA	None	22	None	None
Ch.A DMA Ch.3 Half-Duplex Ch.B No DMA	None	33	None	None
Ch.B DMA Ch.0 Half-Duplex Ch.A No DMA	None	None	None	00
Ch.B DMA Ch.1 Half-Duplex Ch.A No DMA	None	None	None	11
Ch.B DMA Ch.2 Half-Duplex Ch.A No DMA	None	None	None	22
Ch.B DMA Ch.3 Half-Duplex Ch.A No DMA	None	None	None	33

Two DMA Channels Selected

Option	E4	E5	E6	E7
Ch.A DMA Ch.1 Half-Duplex Ch.B DMA Ch.3 Half-Duplex	None	11	None	33
Ch.A DMA Ch.0 Half-Duplex Ch.B DMA Ch.2 Half-Duplex	None	00	None	22

Full Duplex Channel A and B with four DMA Channels

Option	E4	E5	E6	E7
Ch.A DMA Ch.1 Receive Data	33	11	22	00
Ch.A DMA Ch.3 Transmit Data				
Ch.B DMA Ch.0 Receive Data				
Ch.B DMA Ch.2 Transmit Data				

Full Duplex Channel A only

Option	E4	E5	E6	E7
Ch.A DMA Ch.1 Receive Data	33	11	None	None
Ch.A DMA Ch.3 Transmit Data				

Full Duplex Channel B only

Option	E4	E5	E6	E7
Ch.B DMA Ch.1 Receive Data	None	None	33	11
Ch.B DMA Ch.3 Transmit Data				

DMA Enable Header E2

Header E2 selects whether the DMA tri-state drivers are enabled permanently, disabled permanently, or whether the DMA enable control port bit is used to enable the DMA hardware request and acknowledge signals. Moving the jumper to position 'N' disables the drivers and no DMA can be performed.

Note: The power on reset signal resets or disables the DMA software enable signal.

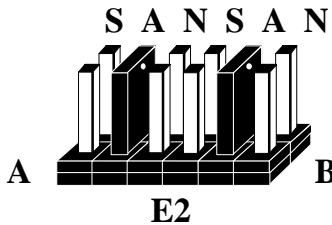


Figure 5 - DMA Enable Header E2

S	Selects Software Enable Channel A
A	Selects Always Enable Channel A
N	Selects No DMA Channel A
S	Selects Software Enable Channel B
A	Selects Always Enable Channel B
N	Selects No DMA Channel B

Note: Please refer to section 4 for software bit definitions and examples of DMA driver control.

IRQ Selection Header E3

Header E3 selects the interrupt request (IRQ) line for the card. If no interrupt is desired, remove the jumper.

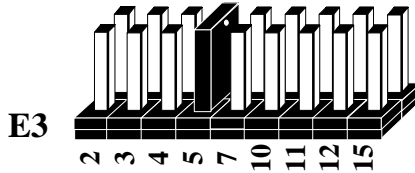


Figure 6 - IRQ Header E3

IRQ Mode Header E1

Header E1 'N' indicates the (N)ormal, single interrupt mode. Position 'M' indicates the inclusion of a 1K ohm pull-down resistor required on one port when sharing interrupts with another card. For shared interrupt mode, set one board to 'M' and the other(s) with the jumper removed. This mode allows more than one board to access a single IRQ. Position 'T' on E1 enables the **DMA Terminal Count Interrupt**. Setting this jumper allows the selected DMA channel to generate an interrupt once the **DMA Terminal Count** has been reached. See Section 4 for the status bit (TC STAT) position and refer to the toolkit disk for software examples.

Note: When using multiple cards on one IRQ in shared mode, be sure that only one port has the 'M' jumper set, providing the necessary pull-down resistor.



Figure 7 - IRQ Mode Header

Installation

The **OMG-ACB-530** can be installed in any of the PC expansion slots. The **OMG-ACB-530** contains several jumper straps for each port, which must be set for proper operation.

1. Turn off PC power. Disconnect the power cord.
2. Remove the PC case cover.
3. Locate two available slots and remove the blank metal slot covers.
4. Install the Channel B cable into Box Header E4. This cable is keyed to prevent improper installation. Gently insert the **OMG-ACB-530** into the slot. Make sure that the adapter is seated properly. Attach the Channel B cable to the adjacent slot with the retaining screw. (If Channel B of the **OMG-ACB-530** is not used, the adapter cable is not required).
5. Replace the cover.
6. Connect the power cord.

Installation is complete.

Cabling Options

The **OMG-ACB-530** has a number of cabling options available. These options include:

- **CA-104** - This cable provides a 6' extension for use with RS-530/422
- **CA-107** - This cable provides a simple interface to the RS-449, DB-37 type connector. RS-530 was designed as a replacement for RS-449.

Technical Description

The **OMG-ACB-530** utilizes the Zilog 85230 Enhanced Serial Communications Controller (ESCC). This chip features programmable baud rate, data format and interrupt control, as well as DMA control. Refer to the ESCC Users Manual for details on programming the 85230 ESCC chip.

Features

- Two channels of sync/async communications using 85230 chip
- DMA supports data rate greater than 1 million bits per second (bps)
- Selectable Port Address, IRQ level (2/9, 3, 4, 5, 7, 10, 11, 12, 15)
- Selectable DMA channels (0, 1, 2, 3)
- EIA-530/422 interface with full modem control supports TD, RD, RTS, CTS, DSR, DCD, DTR, TXC, RXC, LL, RL, TM, TSET signals
- Jumper options for clock source and Input / Output modes
- Software programmable baud rate

Internal Baud Rate Generator

The baud rate of the ESCC is programmed under software control. The standard oscillator supplied with the board is 7.3728 MHz. However, other oscillator values can be substituted to achieve different baud rates.

Programming the OMG-ACB-530

Control/Status Port

The **OMG-ACB-530** occupies eight **Input/Output (I/O)** addresses. The **ESCC** chip uses the first four, while the fifth address (**Base+4**) is the address of the on-board **Control/Status Port**. This port is used to set the **Data Terminal Ready (DTR)**, **Remote Loopback (RL)**, **Local Loopback (LL)** signals, and to enable or disable **DMA** under program control, and to monitor the **Data Set Ready (DSR)** input signals from the modem.

Bit	Output Port Bits	Input Port Bits
0	DTR A 1=On, 0=Off	DSR A 1=Off, 0=On
1	DTR B 1=On, 0=Off	DSR B 1=Off, 0=On
2	LL A 1=On, 0=Off	TM A 1=Off, 0=On
3	RL A 1=On, 0=Off	ESCC INT 1=Off, 0=On
4	LL B 1=On, 0=Off	TM B 1=Off, 0=On
5	RL B 1=On, 0=Off	TC STAT 1=Off, 0=On
6	CH. B DMA Enable ESCC CH.B 1=On, 0=Off	Ch.B DMA 1=Off, 0=On
7	CH. A DMA Enable ESCC CH.A 1=On, 0=Off	Ch.A DMA 1=Off, 0=On

Software Examples

Function	Program Bits
Turn On CH.A DTR	Out (Base+4), XXXX XXX1
Turn On CH.B DTR	Out (Base+4), XXXX XX1X
Turn Off CH.A DTR	Out (Base+4), XXXX XXX0
Turn Off CH.B DTR	Out (Base+4), XXXX XX0X
Turn On CH.A LL	Out (Base+4), XXXX X1XX
Turn On CH.B LL	Out (Base+4), XXX1 XXXX
Turn On CH.A RL	Out (Base+4), XXXX 1XXX
Turn On CH.B RL	Out (Base+4), XX1X XXXX
Turn Off CH.A LL	Out (Base+4), XXXX X0XX
Turn Off CH.B RL	Out (Base+4), XX0X XXXX
Enable DMA Drivers	Out (Base+4), 1XXX XXXX
Disable DMA Drivers	Out (Base+4), 0XXX XXXX
Test CH.A DSR	In (Base+4), Mask=0000 0001
Test CH.B DSR	In (Base+4), Mask=0000 0010
Test CH.A TM	In (Base+4), Mask=0000 0100
Test CH.B TM	In (Base+4), Mask=0001 0000

DMA Terminal Count

The **OMG-ACB-530** can be setup to operate using a polling method, interrupts, or system DMA. The most efficient method is a combination of DMA and interrupts. The **OMG-ACB-530** has been optimized to generate an interrupt at the end of a DMA transfer. This will allow for DMA initialization and buffer management to take place at interrupt time and provide a virtually seamless communication channel. If the 'T' option on header E1 is selected, an onboard latch will be set when Terminal Count for the selected DMA channel(s) is reached. This latch will cause an interrupt to be generated and program execution will be transferred to the application Interrupt Service Routine (ISR). The DMA Terminal Count Interrupt condition should be reset from the ISR by writing to BASE+5. The value that is written to this I/O location is irrelevant. If your application or driver is interrupting on multiple conditions, reading the Status Register located at Base+4 will determine the source of the interrupt (ESCC or DMA Terminal Count generated). Bit D3 in the Status Port corresponds to a ESCC generated interrupt and bit D5 corresponds to an interrupt generated by the end of a DMA transfer. Bit D3 can only be reset by polling the ESCC to determine the interrupt source and required action necessary to reset the interrupt. Please refer to the Software Toolkit and the 85230 Technical Manual for details and examples on interrupt driven and DMA programming examples.

Connector P1 and P2 Pin Assignments

Signal		Name	Pin #	Mode
GND		Ground	7	
RDB	RX+	Receive Positive	16	Input
RDA	RX-	Receive Negative	3	Input
CTSB	CTS+	Clear To Send Positive	13	Input
CTSA	CTS-	Clear To Send Negative	5	Input
DSRB	DSR+	Data Set Ready Positive	22	Input
DSRA	DSR-	Data Set Ready Negative	6	Input
DCDB	DCD+	Data Carrier Detect Positive	10	Input
DCDA	DCD	Data Carrier Detect Negative	8	Input
TDB	TX+	Transmit Positive	14	Output
TDA	TX-	Transmit Negative	2	Output
RTSB	RTS+	Request To Send Positive	19	Output
RTSA	RTS-	Request To Send Negative	4	Output
DTRB	DTR+	Data Terminal. Ready Positive	23	Output
DTRA	DTR-	Data Terminal Ready Negative	20	Output
TXCB	TXC+	Transmit Clock Positive	12	Input
TXCA	TXC-	Transmit Clock Negative	15	Input
RXCB	RXC+	Receive Clock Positive	9	Input
RXCA	RXC-	Receive Clock Negative	17	Input
TSETB	TSET+	Terminal Timing Positive	11	Output
TSETA	TSET-	Terminal Timing Negative	24	Output
LL		Local Loop-Back	18	Output
RL		Remote Loop-Back	21	Output
TM		Test Mode	25	Input

RS-530/422/485 Line Termination

Typically, each end of the RS-530/422/485 bus must have line-terminating resistors. A 100-ohm resistor is across each RS-530/422/485 input in addition to a 1K ohm pull-up/pull-down combination that biases the receiver inputs.

The RS-530 specification calls for a 100-ohm 1/2-watt resistor between the signal ground and the chassis ground. On the IBM PC, these two grounds are already connected together, therefore this resistor is omitted.

Specifications

Environmental Specifications

Specification	Operating	Storage
Temperature Range	0° to 50° C (32° to 122° F)	-20° to 70° C (-4° to 158° F)
Humidity Range	10 to 90% R.H. Non-Condensing	10 to 90% R.H. Non-Condensing

Power Consumption

Supply line	+5 VDC
Rating	900 mA

Mean Time Between Failures (MTBF)

Greater than 150,000 hours. (Calculated)

Physical Dimensions

Board length	5.8 inches	(14.73 cm)
Board Height including Goldfingers	4.2 inches	(10.66 cm)
Board Height excluding Goldfingers	3.9 inches	(9.91 cm)

Please see Appendix G for board layout and dimensions.

Appendix A - Troubleshooting

An ACB Developers Toolkit Diskette is supplied with the Omega Engineering adapter and will be used in the troubleshooting procedures. By using this diskette and following these simple steps, most common problems can be eliminated without the need to call Technical Support.

1. Identify all I/O adapters currently installed in your system. This includes your on-board serial ports, controller cards, sound cards etc. The I/O addresses used by these adapters, as well as the IRQ (if any) should be identified.
2. Configure your Omega Engineering adapter so that there is no conflict with currently installed adapters. No two adapters can occupy the same I/O address.
3. Make sure the Omega Engineering adapter is using a unique IRQ. While the Omega Engineering adapter does allow the sharing of IRQ's, many other adapters (i.e. SCSI adapters & on-board serial ports) do not. The IRQ is typically selected via an on-board header block. Refer to the section on Card Setup for help in choosing an I/O address and IRQ.
4. Make sure the Omega Engineering adapter is securely installed in a motherboard slot.
5. Use the supplied diskette and User Manual to verify that the Omega Engineering adapter is configured correctly. The supplied diskette contains a diagnostic program 'SSDACB' that will verify if an adapter is configured properly. Refer to the 'UTIL.txt' file found in the \UTIL sub-directory on the supplied diskette for detailed instructions on using 'SSDACB'.
6. The following are known I/O conflicts:
 - 3F8-3FF is typically reserved for COM1:
 - 2F8-2FF is typically reserved for COM2:
 - 3E8-3EF is typically reserved for COM3:
 - 2E8-2EF is typically reserved for COM4:.. This is a valid setup option for the **OMG-ACB-530**. However, since only 10 address lines are actually decoded, a possible conflict with an advanced video card emulating the IBM XGA adapter (8514 register set) may occur.

Appendix B - How To Get Assistance

Please refer to Appendix A - Troubleshooting prior to calling Technical Support.

1. Read this manual thoroughly before attempting to install the adapter in your system.
2. When calling for technical assistance, please have your user manual and current adapter settings. If possible, please have the adapter installed in a computer ready to run diagnostics.
3. Omega Engineering maintains a home page on the World Wide Web, www.omega.com, providing utilities and new product information.
4. Technical support is available Monday to Friday from 8:30 a.m. to 6:00 p.m. Eastern time. Technical support can be reached at (800) 826-6342 x2295.

RETURN AUTHORIZATION MUST BE OBTAINED FROM OMEGA ENGINEERING BEFORE RETURNED MERCHANDISE WILL BE ACCEPTED. AUTHORIZATION CAN BE OBTAINED BY CALLING OMEGA ENGINEERING AND REQUESTING A RETURN MERCHANDISE AUTHORIZATION (RMA) NUMBER.

Appendix C - Electrical Interface

RS-422

The RS-422 specification defines the electrical characteristics of balanced voltage digital interface circuits. RS-422 is a differential interface that defines voltage levels and driver/receiver electrical specifications. On a differential interface, logic levels are defined by the difference in voltage between a pair of outputs or inputs. In contrast, a single ended interface, for example RS-232, defines the logic levels as the difference in voltage between a single signal and a common ground connection. Differential interfaces are typically more immune to noise or voltage spikes that may occur on the communication lines. Differential interfaces also have greater drive capabilities that allow for longer cable lengths. RS-422 is rated up to 10 Megabits per second and can have cabling 4000 feet long. RS-422 also defines driver and receiver electrical characteristics that will allow 1 driver and up to 32 receivers on the line at once. RS-422 signal levels range from 0 to +5 volts. RS-422 does not define a physical connector.

RS-530

RS-530 (a.k.a. EIA-530) compatibility means that RS-422 signal levels are met, and the pin-out for the DB-25 connector is specified. The Electronic Industry Association (EIA) created the RS-530 specification to detail the pin-out, and define a full set of modem control signals that can be used for regulating flow control and line status. The RS-530 specification defines two types of interface circuits, **Data Terminal Equipment (DTE)** and **Data Circuit-Terminating Equipment (DCE)**. The Omega Engineering adapter is a DTE interface.

RS-449

RS-449 (a.k.a. EIA-449) compatibility means that RS-422 signal levels are met, and the pin-out for the DB-37 connector is specified. The EIA created the RS-449 specification to detail the pin-out, and define a full set of modem control signals that can be used for regulating flow control and line status.

RS-485

RS-485 is backwardly compatible with RS-422; however, it is optimized for partyline or multi-drop applications. The output of the RS-422/485 driver is capable of being **Active** (enabled) or **Tri-State** (disabled). This capability allows multiple ports to be connected in a multi-drop bus and selectively polled. RS-485 allows cable lengths up to 4000 feet and data rates up to 10 Megabits per second. The signal levels for RS-485 are the same as those defined by RS-422. RS-485 has electrical characteristics that allow for 32 drivers and 32 receivers to be connected to one line. This interface is ideal for multi-drop or network environments. RS-485 tri-state driver (not dual-state) will allow the electrical presence of the driver to be removed from the line. The driver is in a tri-state or high impedance condition when this occurs. Only one driver may be active at a time and the other driver(s) must be tri-stated. The output modem control signal **Request to Send (RTS)** controls the state of the driver. Some communication software packages refer to RS-485 as RTS enable or RTS block mode transfer. RS-485 can be cabled in two ways, two wire and four wire mode. Two wire mode does not allow for full duplex communication, and requires that data be transferred in only one direction at a time. For half-duplex operation, the two transmit pins should be connected to the two receive pins (Tx+ to Rx+ and Tx- to Rx-). Four wire mode allows full duplex data transfers. RS-485 does not define a connector pin-out or a set of modem control signals. RS-485 does not define a physical connector.

Appendix D - Direct Memory Access

In many instances it is necessary to transmit and receive data at greater rates than would be possible with simple port I/O. In order to provide a means for higher rate data transfers, a special function called **Direct Memory Access (DMA)** was built into the original IBM PC. The DMA function allows the **OMG-ACB-530** (or any other DMA compatible interface) to read or write data to or from memory without using the Microprocessor. This function was originally controlled by the Intel 8237 DMA controller chip, but may now be a combined function of the peripheral support chip sets (i.e. Chips & Technology or Symphony chip sets).

During a DMA cycle, the DMA controller chip is driving the system bus in place of the Microprocessor, providing address and control information. When an interface uses DMA, it activates a DMA request signal (DRQ) to the DMA controller, which in turn sends a DMA hold request to the Microprocessor. When the Microprocessor receives the hold request it will respond with an acknowledge to the DMA controller chip. The DMA controller chip then becomes the owner of the system bus providing the necessary control signals to complete a Memory to I/O or I/O to Memory transfer. When the data transfer is started, an acknowledge signal (DACK) is sent by the DMA controller chip to the **OMG-ACB-530**. Once the data has been transferred to or from the **OMG-ACB-530**, the DMA controller returns control to the Microprocessor.

To use DMA with the **OMG-ACB-530** requires a thorough understanding of the PC DMA functions. The ACB Developers Toolkit demonstrates the setup and use of DMA with several source code and high-level language demo programs. Please refer to the ESCC User's Manual for more information.

Appendix E - Asynchronous and Synchronous Communications

Serial data communications implies that individual bits of a character are transmitted consecutively to a receiver that assembles the bits back into a character. Data rate, error checking, handshaking, and character framing (start/stop bits or sync characters) are pre-defined and must correspond at both the transmitting and receiving ends. The techniques used for serial communications can be divided two groups, *asynchronous* and *synchronous*.

When contrasting asynchronous and synchronous serial communications, the fundamental differences deal with how each method defines the beginning and end of a character or group of characters. The method of determining the duration of each bit in the data stream is also an important difference between asynchronous and synchronous communications. The remainder of this section is devoted to detailing the differences between character framing and bit duration implemented in asynchronous and synchronous communications.

Asynchronous Communications

Asynchronous communications is the standard means of serial data communication for PC compatibles and PS/2 computers. The original PC was equipped with a communication or COM: port that was designed around an 8250 Universal Asynchronous Receiver Transmitter (UART). This device allows asynchronous serial data to be transferred through a simple and straightforward programming interface. Character boundaries for asynchronous communications are defined by a starting bit followed by a pre-defined number of data bits (5, 6, 7, or 8). The end of the character is defined by the transmission of a pre-defined number of stop bits (usual 1, 1.5 or 2). An extra bit used for error detection is often appended before the stop bits.

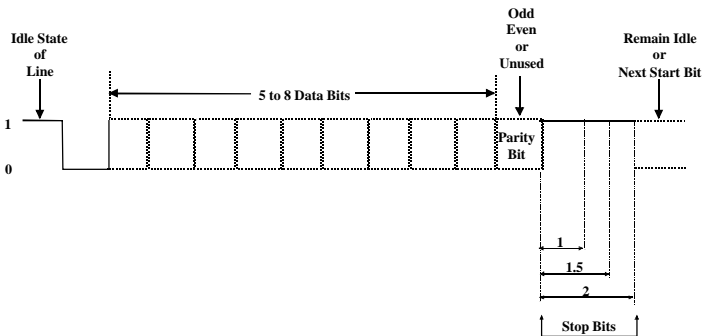


Figure 8 - Asynchronous Communications Bit Diagram

This special bit is called the parity bit. Parity is a simple method of determining if a data bit has been lost or corrupted during transmission. There are several methods for implementing a parity check to guard against data corruption. Common methods are called (E)ven Parity or (O)dd Parity. Sometimes parity is not used to detect errors on the data stream. This is referred to as (N)o parity. Because each bit in asynchronous communications is sent consecutively, it is easy to generalize asynchronous communications by stating that each character is wrapped (framed) by pre-defined bits to mark the beginning and end of the serial transmission of the character. The data rate and communication parameters for asynchronous communications have to be the same at both the transmitting and receiving ends. The communication parameters are baud rate, parity, number of data bits per character, and stop bits (i.e. 9600,N,8,1).

Synchronous Communications

Synchronous Communications is used for applications that require higher data rates and greater error checking procedures. Character synchronization and bit duration are handled differently than asynchronous communications. Bit duration in synchronous communications is not necessarily pre-defined at both the transmitting and receiving ends. Typically, in addition to the data signal, a clock signal is provided. This clock signal will mark the beginning of a bit cell on a pre-defined transmission. The source of the clock is predetermined and sometimes multiple clock signals are available. For example, if two nodes want to establish synchronous communications, point A could supply a clock to point B that would define all bit boundaries that A transmitted to B. Point B could also supply a clock to point A that would correspond to the data that A received from B. This example demonstrates how communications could take place between two nodes at completely different data rates. Character synchronization with synchronous communications is also very different than the asynchronous method of using start and stop bits to define the beginning and end of a character. When using synchronous communications a pre-defined character or sequence of characters is used to let the receiving end know when to start character assembly.

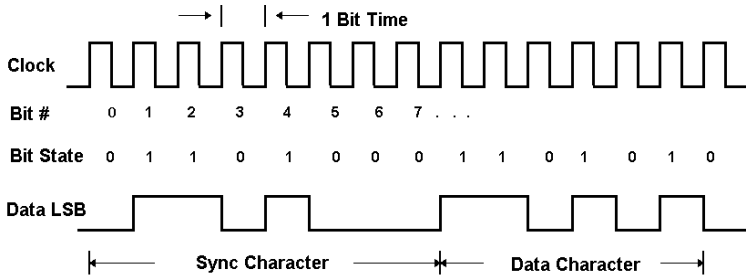


Figure 9 - Synchronous Communications Bit Diagram

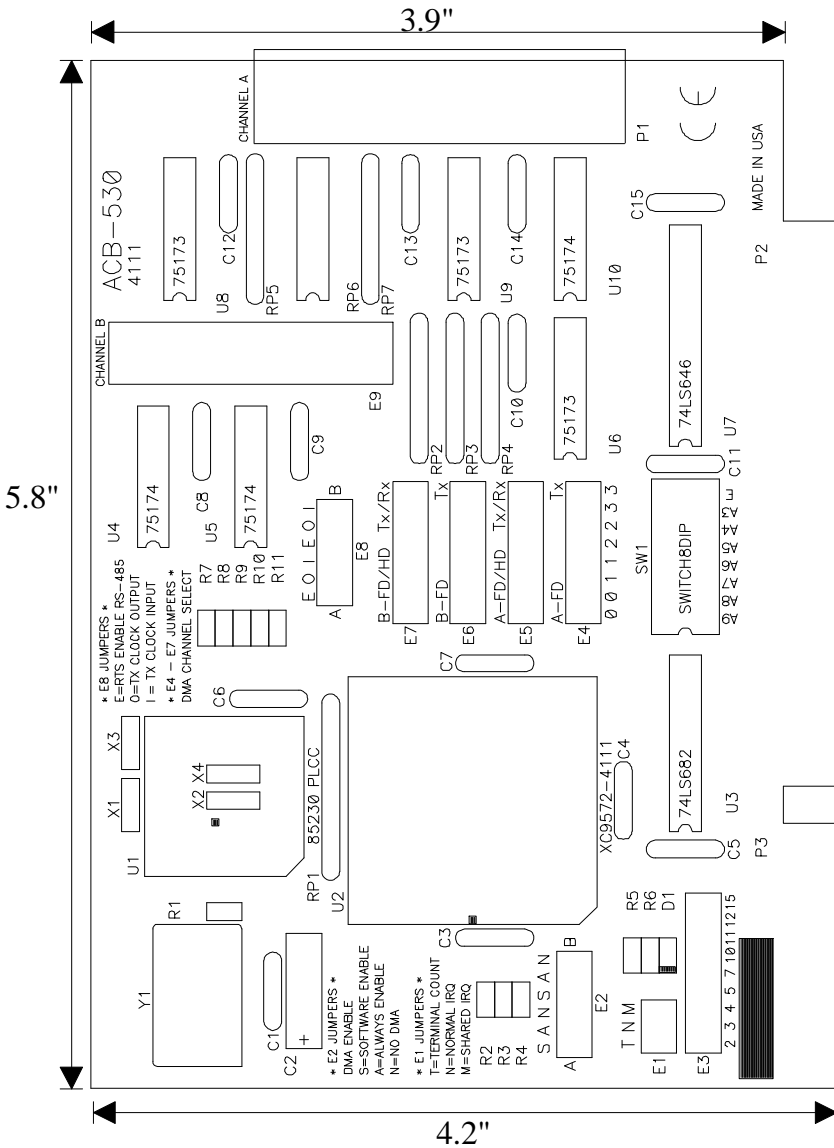
This pre-defined character is called a sync character or sync flag. Once the sync flag is received, the communications device will start character assembly. Sync characters are typically transmitted while the communications line is idle or immediately before a block of information is transmitted. To illustrate with an example, let's assume that we are communicating using eight bits per character. Point A is receiving a clock from point B and sampling the receive data pin on every upward clock transition. Once point A receives the pre-defined bit pattern (sync flag), the next eight bits are assembled into a valid character. The following eight bits are also assembled into a character. This will repeat until another pre-defined sequence of bits is received (either another sync flag or a bit combination that signals the end of the text, e.g., EOT). The actual sync flag and protocol varies depending on the sync format (SDLC, BISYNC, etc.).

For a detailed explanation of serial communications, please refer to the book *Technical Aspects of Data Communications* by John E. McNamara, published by Digital Press (DEC) 1982.

Appendix F - ACB Developer Toolkit Diskette and ACB Resource Kit

The ACB Developer Toolkit diskette provides sample software, a DOS version of the SeaMAC Driver, and technical insight to aid in the development of reliable applications for the ACB family of communication cards. The goal in publishing this collection of source code and technical information is two fold. First, to provide the developer with ample information to develop ACB based applications. Second, to provide a channel for suggestions into the technical support efforts. The ACB Resource Kit provides a detailed overview of the ACB product line and is available at your request. Topics concerning applications and integration are covered to provide a complete overview of the versatile ACB family. During ACB development, if any questions, comments, or suggestions arise, please contact Technical Support at the numbers listed at the end of this manual.

Appendix G - Silk-Screen



Appendix H - Compliance Notices

Federal Communications Commission Statement

FCC - This equipment has been tested and found to comply with the limits for Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in such case the user will be required to correct the interference at his own expense.

EMC Directive Statement



Products bearing the CE Label fulfill the requirements of the EMC directive (89/336/EEC) and of the low-voltage directive (73/23/EEC) issued by the European Commission.

To obey these directives, the following European standards must be met:

- **EN55022 Class A** - 'Limits and methods of measurement of radio interference characteristics of information technology equipment'
- **EN50082-1** - 'Electromagnetic compatibility - Generic immunity standard' Part 1: Residential, commercial and light industry
- **EN60950 (IEC950)** - 'Safety of information technology equipment, including electrical business equipment'

Warning

This is a Class A Product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

Always use cabling provided with this product if possible. If no cable is provided or if an alternate cable is required, use high quality shielded cabling to maintain compliance with FCC/EMC directives.

Warranty

Omega Engineering, Inc. warrants this product to be in good working order for a period of one year from the date of purchase. Should this product fail to be in good working order at any time during this period, Omega Engineering will, at its option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Omega Engineering assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Omega Engineering will not be liable for any claim made by any other related party.

RETURN AUTHORIZATION MUST BE OBTAINED FROM OMEGA ENGINEERING BEFORE RETURNED MERCHANDISE WILL BE ACCEPTED. AUTHORIZATION CAN BE OBTAINED BY CALLING OMEGA ENGINEERING AND REQUESTING A RETURN MERCHANDISE AUTHORIZATION (RMA) NUMBER.

Omega Engineering, Incorporated
One Omega Drive
PO Box 4047
Stamford, CT 06907
(800)826-6342 FAX: (203)359-7990
email: Internet: das@omega.com
Web Site: www.omega.com

Technical Support is available from 8:30 a.m. to 6 p.m. Eastern time.
Monday - Friday

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